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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :
H04L 7/00, 7/02

A2

(11) International Publication Number: WO 98/04063

(43) International Publication Date: 29 January 1998 (29.01.98)

(21) International Application Number: PCT/SE97/01168

(22) International Filing Date: 27 June 1997 (27.06.97)

(30) Priority Data:
9602823-8 19 July 1996 (19.07.96) SE

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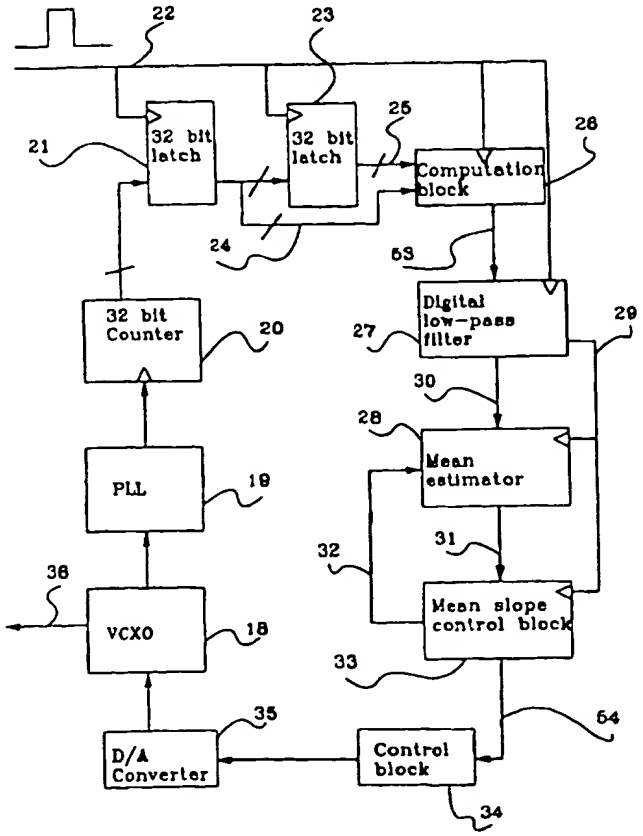
(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ARIPO patent (GH, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published
Without international search report and to be republished upon receipt of that report.

(54) Title: A METHOD, AN APPARATUS AND A NETWORK FOR CLOCK RECOVERY

(57) Abstract

The present invention relates to a method, an apparatus and a network for recovery of the clock of a constant bit-rate service transported over a packet-switched network. The invention measures the inter-arrival time, W_n, between consecutive packages, filter the results through a noise reduction function (27, 52) and calculates a mean value (28) of the inter-arrival times. If the derivative (38) of the mean values is less than an error level (39) for a specified number of times (42), the frequency (18) with which the arrival buffer is polled is adjusted to comply with the frequency with which the CBR service is sent. Whenever the frequency (18) is adjusted a new period for the calculation of the mean values is started. To be able to react faster at start-up, the error level is reduced down to a specified minimum level (45) when the frequency is adjusted.



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A METHOD, AN APPARATUS AND A NETWORK FOR CLOCK RECOVERY

FIELD OF THE INVENTION

The present invention relates to a method, an apparatus and a network for recovering the clock of a constant bit-rate service, which is transported over an packet-switched network.

BACKGROUND OF THE INVENTION

Through WO, A1, 95/33320 it is known to recover a clock signal by periodically sample a buffer fill level and adjusting a clock frequency to achieve a steady-state mean of the buffer fill level or its derivative.

Through WO, A1, 95/22233 it is known to submit to the first packet, of a sequence of packets, a predetermined delay after that the fill level of a delay buffer is monitored and subsequent packages are submitted to a variable delay to maintain the fill level of said buffer to minimise the risk of over- or underflow of said buffer.

In IEEE 1988 ref. CH2535-3/88/0000-1468 a time-averaging method and an optimal control method is presented.

SUMMARY OF THE INVENTION

To be able to transport a synchronous service with a CBR (Constant Bit-Rate) over an asynchronous packet-switched network there must exist some means to match the clock frequency at the receiving end to the clock frequency at the transmitting end. This is essential so that buffers on the receiving side does not drain or overflow. If the clock frequency at the receiving side is a fraction too fast the frequency with which the receiving buffer is emptied is greater than the frequency with which it is filled, which eventually will lead to a temporary stop of the CBR service. If, on the other hand, the receiving clock is too slow the receiving buffer will overflow and data will be lost.

One way of achieving same clock frequency on both transmitting and receiving side is to supervise the periodic arrivals of the CBR traffic and adjust the receiving clock frequency accordingly. This is, however, not a straight-forward task since each cell is submitted to individual delays, so called cell jitter.

The cell jitter is the result of the multiplexing and queuing in the packet-switched network. The cell queuing in a switch introduce a delay which is related to the traffic congestion the switch is experiencing. The traffic congestion, in turn, depends on the traffic from other sources and their inter-arrival time distributions. The delay introduced for multiplexing depends on the multiplexing policies of the switches the cell passes on its way to the receiver.

One major problem with transporting CBR services over packet-switched networks is therefore to find a stable and secure way of recovering the clock-signal at the receiving end.

Another problem which the present invention solves is to avoid excessive clock wander.

Another problem which this invention solves is to achieve rapid convergence times for the regulation of the clock frequency.

Another problem which the invention solves is to avoid destructive effects of cell-loss on the regulation.

The object with the present invention is to secure a safe transport of a CBR service over a packet-switched network.

Another objective with the present invention is to recover the clock of a CBR service transported over a packet-switched network.

The present invention solves the problem with recovering the clock signal of a CBR service which is transported over a

packet-switched network by filtering the measured packet inter-arrival times, taking the mean-value of the result over a certain period, depending on the value of the derivative, or the value of several consecutive derivatives, of the mean-values adjusting the period used for taking the mean-values and depending on the value of the derivative adjusting the clock frequency for fetching cells from the receive buffer.

In more detail the proposed solution measures the time between two consecutive cell arrivals. By continuously measuring this time, and from each value subtract the expected inter-arrival time, a Series of samples, with the expected mean value of zero, is produced. This series of samples is passed through a filter in order to reduce the noise. From the filter the modified series is passed to a Mean estimator. The Mean estimator takes the mean-value, from a start sample and up to the current sample. That is, for every new sample the Mean estimator adds the value of the sample to a stored sum and takes the mean of this sum. This will result in a series of samples from the Mean estimator, this series is supplied to a Mean slope control block which takes the derivative of the supplied series and depending on the value of the derivative, or the value of several consecutive derivatives, resets the sum of the Mean estimator to zero and supplies information to adjust the clock frequency for fetching data from the receiving buffer.

The advantage with the invention is that it has a fast convergence time.

Another advantage is that the invention is not sensitive to rapid change in network traffic load.

Another advantage is that the invention is not sensitive to loss or misinserted cells.

Another advantage is that the invention can be implemented on a IC (Integrated Circuit) or with a DSP (Digital Signal Processing) device and only a few extra components.

The invention will now be described with help of preferred embodiments and with references to the supplied drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows the principal of sending CBR service over a packet-switched network.

Figure 2 shows a block diagram of the principals of receiving CBR data.

Figure 3 shows a block diagram of the clock recovery system in figure 2 according to the invention.

Figure 4 shows a flow diagram of the Mean slope control block in figure 3 according to the invention.

Figure 5 shows an implementation of the digital low-pass filter in figure 4 according to the invention.

Figure 6 shows buffer occupancy results from a simulation according to the invention.

Figure 7 shows clock frequency results from a simulation according to the invention.

Figure 8 shows output from the Mean estimator from a simulation according to the invention.

BRIEF DESCRIPTION OF THE PREFERRED EMBODIMENTS

In figure 1 two Narrow Band Terminals 1 are sources of CBR services 5. They need to establish a virtual circuit to communicate with each other over the Packet-Switched Network 3. In most cases the Packet-Switched Network 3 will be an ATM (Asynchronous Transfer Mode) network. This is of course not

always so and the Packet-Switched Network 3 can be of many other types, for instance X.25, Token Ring, Ethernet, etc. In this embodiment the Packet-Switched Network 3 is an ATM network.

Since the transmission and the switching in the ATM network introduces a variable transfer delay it is more suitable for transmission of bursty data than data from a CBR service 5. For this reason an adaptation for the transport of the CBR traffic 5 is performed by the CE (Circuit Emulation functionality) 2. The CE 2 performs necessary adaptations to emulate all the services of a T1/E1 circuit that is virtually connected to the remote Narrow Band Terminal 1. If the ATM network 3 is seen as the future broadband network (B-ISDN, Broadband-Integrated Services Digital Network) and the Narrow Band Terminals 1 operates in the existing narrowband network (N-ISDN, Narrowband-Integrated Services Digital Network) the CE 2 can be seen as providing the integration, being a inter-working unit, between these two networks. The CE 2 interfaces, on the broadband side, the ATM cells and, on the narrowband side, the synchronous bitstream from the CBR signal 5. The CBR signal 5 is segmented, by the CE 2, into 376 bits units, which is equal to 47 octets and then mapped into the payload field of an ATM cell. The cell is then routed through the ATM network 3.

One of the services that shall be provided by the CE 2 is the recovery of the remote source clock information 4. This is essential to the proper delivery of the CBR service traffic since any frequency errors in the clock controlling the destination buffer operation results in buffer over- or underflow. Only little is known about the ATM cell jitter, caused by queuing and multiplexing of the ATM cells in the ATM network, also called CDV (Cell Delay Variation), beyond that the average cell delay is constant, assuming that the cell loss probability is negligible.

All previously known clock recovery methods start from this hypothesis. The present invention starts from a weaker hypothesis that allow it to be functional even if the cell loss probability is not negligible.

In figure 2 is a functional block diagram for the receiving side of a CE 2 shown. The ATM cells are received from the ATM network 11 through the ATM adapter 9 and processed in the AAL1 (ATM Adaptation Layer 1) 8. The AAL1 block 8 terminates the AAL1 protocol and extracts from each cell 47 octets which corresponds to 376 bits of the CBR service traffic. Each time a valid ATM cell is received in the AAL1 block 8 a signal 14 is sent to the Clock Recovery System 10. The output of the Clock Recovery System 10 is the clock 15 used to re-generate the CBR service traffic from the cells to the 2 Mbit/s line 16. This 2 Mbit/s stream is passed to the Narrowband Terminal through the Line I/F transceiver block 7.

In figure 3 is a detailed functional block diagram of the Clock Recovery System 10 in figure 2 shown. When a valid ATM cell is received in the AAL1 block 8 in figure 2 a signal is raised which arrives on line 22 in figure 3 and applied to a first 32-bit latch 21, a second 32-bit latch 23, an computation block 26 and a Digital low-pass filter 27. The clock source in this embodiment is a VCXO quartz voltage controlled oscillator 18 with frequency f_1 36. It has a high degree of stability in frequency in respect to the applied voltage and temperature. Its output frequency, f_1 36, can be assumed to be constant for a given input control voltage. The generated frequency f_1 36 is applied to a PLL (Phased Locked Loop) 19 used to multiply the VCXO frequency f_1 with a constant M. This multiplication is done to be able to measure the cell inter-arrival time with enough accuracy. The cell inter-arrival time is measured by applying the $M \times f_1$ clock to a free running 32-bit counter 20. The output of this counter 20 is latched from the first 32-bit

latch 21 when a cell is received. The preceding value X_{n-1} 25 of the 32-bit counter 20 is stored in the second 32-bit latch 23 and is fed to the computation block 26 together with the current value X_n 24.

By letting M cells interarrival times be accumulated in the 32-bit counter the need for the PLL can be eliminated.

Let's call the unknown transmitter clock f_t. Each cell is transmitted when 47 octets, corresponding to $47 \times 8 = 376$ bits, has been stored in the cell. Therefore the cell generation period is:

$$T_c = \frac{376}{f_t}$$

Let's suppose that the ATM network introduces a constant delay in the transport of each cell. With this assumption the cell inter-arrival time is constant and equal to T_c. In this case we can evaluate the number of counted periods w_n, which is directly corresponding to the inter-arrival time, that represent the T_c value:

$$w_n = |x_n - x_{n-1}| = M \times f_s \times T_c = M \times f_s \times \frac{376}{f_t} = M \times 376 \times \frac{f_s}{f_t}$$

The fractional residual part of the result is accumulated by the counter 20 and counted as a unit when a sufficient number of cells has been received. In this way the precision of the timing measurement is maintained and very low clock differences can be measured. If the two frequencies f_s and f_t are equal the expected value for w_n is:

$$\overline{w_n} = M \times 376$$

To obtain a value that is equal to zero when f_s and f_t are equal the following calculation is performed by the computation block 26 when a cell is received:

$$y_n = w_n - \overline{w_n} = (x_n - x_{n-1}) - (M \times 376)$$

The output y_n 53 from the computation block 26 is applied to a digital low-pass filter 27 with a sampling period equal to T_c. The purpose of the digital low-pass filter 27 is to integrate the result of the previous blocks and to reduce the effect of the jitter in the CDV. The digital low-pass filter 27 accept a new sample and generates a new value z_n 30 when a new cell arrives.

Instead of using a μIIR digital low pass filter, a FIR (Finite Impulse Respons) filter can be used. The FIR filter can be optimised to, in an adaptive way, have a certain amount of noise.

From the digital low-pass filter a clock signal 29 is supplied to the Mean estimator 28 and the Mean slope control block 33. Depending on the implementation of the digital low-pass filter 27 the clock signal 22 and the clock signal 29 can be different.

The output z_n 30 of the digital low-pass filter 27 is applied to a Mean estimator 28. This block performs the mean evaluation of the received z_n 30 producing a sequence of output values m_k 31 according to the following formula:

$$m_k = \frac{\sum_{n=s}^{k-1} z_n}{k-s}$$

where s is a start position for the mean-value calculation. This block can be reset by zeroing the accumulated sum and setting $s=k$. The m_k sequence 31 is applied to the Mean slope control block 33 which is responsible for the decision on how many z_n 30 samples the Mean estimator block 28 must accumulate to obtain a good estimation of the mean cell inter-arrival time. The block also performs the evaluation of the correction value

e_i 54 to be applied to the control block 34. The value e_i 54 is maintained stable until a new value is calculated and supplied to the Control block 34. The Control block 34 maintains a value d_i which is supplied to a D/A Converter 35 which converts the value d_i to a voltage supplied to the VCXO clock 18. The Mean slope control block 33 also determines when to reset 32 the Mean estimator 28. When a new e_i 54 value is supplied to the Control block 34 a new d_i value is computed according to:

$$d_i = d_{i-1} + e_i$$

which new d_i value will, through the D/A Converter 35, change the voltage and thereby the frequency of the VCXO clock 18.

In figure 4 a flow diagram of the Mean slope control block 33 in figure 3 is shown. When a new m_k value arrives 37, the derivative c_k 38 of the m_k sequence is computed according to:

$$c_k = \left| \frac{m_k - m_{k-1}}{m_k} \right|$$

A test 39 is performed on the value of c_k. If c_k is less than or equal to an error level, *err*, a counter, *count*, is increased 41. If c_k is greater than *err*, *count* is set to zero 40. If the test 42 $count \geq Maxcnt$ is true a new e_i value is computed 43 according to:

$$e_i = m_k \times Gain$$

and is applied 46 to the control block 34 in figure 3. The Mean estimator is also reset through 46.

By waiting *Maxcnt* number of times before computing a new e_i enough samples has been collected by the Mean estimator 28 to be able to calculate a good enough mean value. This in turn means that the m_k value used to calculate the e_i value will not fluctuate too much. This is in accordance with the asymptotic convergence property of the Mean estimator 28. This property is

reflected by the slope of the m_i sequence that asymptotically tends to zero.

Every time an e_i value is computed the *err* value is reduced 45 down to a predefined minimum error level, *Minerr* 44. This is to achieve rapid convergence at start-up and better precision when the system is stable. By resetting the Mean estimator 28 after each correction the effect of cell loss or misinsertion on the system convergence is removed.

Figures 6, 7 and 8 shows the results of simulations done according to the invention. The simulations has been executed by using a VERILOG system description. The following values has been used in the simulation:

Traffic inter-arrival time, mean value:	183.5937 µs
Traffic inter-arrival time, variance:	20 µs
Initial *err* value:	$1E^{-3}$
Minerr value:	$1E^{-6}$
M value:	8
VCXO frequency:	2.048 Mhz
The *Gain* value:	$0.05 \times \left(\frac{1}{376 \times M \times 2.048} \right)$
Maxcnt value:	16

The simulated traffic source is the output of an ATM switch with a load of 90% having an output speed of 155 Mbit/s.

Figure 6 represent the AAL1 buffer size. The figure qualify the behaviour of the invention, as can be seen the buffer size is stable.

Figure 7 represent the clock generated from the VCXO 18. While figure 8 shows the output of the Mean estimator 28. Note the asymptotic convergence of the m_i sequence.

The invention is of course not limited to the above described and on the drawings shown preferred embodiments, but can also be modified in agreeement with the supplied claims.

CLAIMS

1. A method for recovery of the clock frequency of a constant bit-rate service carried over a packet-switched network comprising storage means for temporarily storing the data at the receiving end, and a clock frequency (18) with which the data is polled out of said storage means, CHARACTERISED in that a first series of time differences, w_n, between consecutive packet arrivals is computed, that said series of time differences, w_n, is applied to a Mean estimator (28) wherein said Mean estimator comprises means to compute a series of mean values, m_k (31), from said series of time differences, w_n, that each sample in said series of mean values, m_k (31), is calculated over a period T_r, that said series of mean values is applied to a Mean slope control block (33), wherein said Mean slope control block comprises means for computing a series of derivatives, c_k (38), from said series of mean values and depending on the value of said derivative or the values of several consecutive derivatives adjust said clock frequency (18) and said period T_r.

2. A method according to claim 1, CHARACTERISED in that a second series of time differences, y_n, (53) is calculated by subtracting, from each sample in said first series of time differences, w_n, the expected mean value interarrival time.

3. A method according to claim 2, CHARATERISED in that before said Series of mean-values, m_k, (31) is calculated said first or second series of time differences, w_n or y_n (53), is passed through a noise reduction function (27) producing a third series of time differences, z_n (30).

4. A method according to claim 3, CHARACTERISED in that said noise reduction function is performed using a digital low pass filter (52) with a period equal to the expected inter-arrival time, T_c.

5. A method according to claim 3, CHARACTERISED in that said noise reduction function is performed using a finite impulse response filter.

6. A method according to claim 5, CHARACTERISED in that said finite impulse response filter is adaptively optimized for a specific noise level.

7. A method according to claim 3, CHARACTERISED in that for each sample in the first series of time differences, w_n, a new sample of said second series of time differences, y_n, (53) is calculated, a new sample of said third series of time differences, z_n, (30) is calculated, a new sample of said series of mean values, m_k (31), is calculated, and a new sample of said series of derivatives, c_k (38), is calculated.

8. A method according to claim 3, CHARACTERISED in that for each sample in the first series of time differences, w_n, a new sample of said second series of time differences, y_n (53), is calculated and that for a specific number of samples in the first series of time differences, w_n, a new sample of said third series of time diferences, z_n (30), is calculated, a new sample of said series of mean values, m_k (31), is calculated, and a new sample of said series of derivatives, c_k (38), is calculated.

9. A method according to claim 8, CHARACTERISED in that said specific number of samples in said first time series, w_n, is eight.

10. A method according to claim 4, CHARACTERISED in that data passed to said digital low pass filter (52) is passed to a first low pass filter (47), that data from the first low pass filter (47) is applied to a decimator (48), that data from said decimator (48) is applied to a second low pass filter (49) and that said decimator (48) supplies a clock signal

(29, 51) to said Mean estimator (28) and to said Mean slope control block (33).

11. A method according to claim 1, CHARACTERISED in that if the absolute value of a sample in said Series of derivatives, c_k (38), is less than, or equal to, an error level (39) a counter is increased (41), that if said absolute value is greater than said error level (39) said counter is set to zero (40), that if said counter (39,40) is greater than a maxcounter level (42) the clock frequency (18) is adjusted and the period, T_r, over which said mean-values is calculated is adjusted.

12. A method according to claim 11, CHARACTERISED in that if said error level (39) is greater than or equal to a predefined minimum error level (44) said error level is decreased (45).

13. A method according to claim 1 or claim 11, CHARACTERISED in that said clock frequency (18) is adjusted by applying a sample value, c_k (38), of said calculated derivative multiplied by a gain value, Gain (43), to a control block (34) wherein said control block holds a value, d_i, and adds said value, c_k*Gain (43), to said value, d_i, that said value, d_i, is applied to a digital/analog converter (35) and that the output of said digital/analog converter (35) is applied to the clock supplying said clock frequency (18).

14. A method according to claim 1 or claim 11, CHARACTERISED in that each sample in said Series of mean-values, m_k (31), is calculated by adding the current sample value to a sum, adding one to the number of received samples, and dividing the sum with the number of received samples and, depending of the value of said derivative, c_k (38), that said period, T_r, over which said mean values, m_k (31), is calculated is adjusted by setting said sum and said number of samples in said mean estimatior to zero.

15. A method according to claim 1, CHARACTERISED in that said time differences, w_n, is calculated by raising a signal (22) when a packet is received, that the value of a free-running counter (20) with a known frequency is stored (21) when said signal (22) is raised and, that the value, x_{n-1} (25), for the previously arrived packet, of the free-running counter, is subtracted from the value, x_n (24), of the current packet.

16. An apparatus for recovery of the clock frequency of a constant bit-rate service carried over a packet-switched network comprising storage means for temporarily storing the data at the receiving end and a clock (18) arranged to determine the rate of polling data from said storage means, CHARACTERISED in said apparatus comprising means for computing time differences between two consecutive arriving packets (20, 21, 23, 26), means for noise reduction (27, 52), a Mean estimator (28), a Mean slope control block (33) and means for adjusting the frequency (34, 35) with which said clock (18) operates.

17. An apparatus according to claim 16, CHARACTERISED in that said Mean slope control block (33) comprises means for calculating the derivative (38) of the input data, means for adjusting (32, 46) the period over which said Mean estimator (28) is provided for calculating mean values and means for supplying data (46) to said means for adjusting said clock frequency (34, 35).

18. An apparatus according to claim 16, CHARACTERISED in that said means for noise reduction (27) is a digital low pass filter with a period equal to the expected inter-arrival time, T_c.

19. An apparatus according to claim 16, CHARACTERISED in that said means for noise reduction (27) is a finite impulse response filter.

20. An appartus according to claim 18, CHARACTERISED in that said digital low pass filter (27, 52) comprises a first low pass filter (47), a decimator (48) and a second low pass filter (49) and that said decimator (48) comprises means for supplying a clock signal (51) to said Mean estimator (28) and to said Mean slope control block (33).

21. A packet-switched network comprising means for transmitting and receiving a constant bit-rate service between at least two nodes in said network, CHARACTERISED in that said means for transmitting and receiving a constant bit-rate service comprises means for recovery of the constant bit-rate clock (10), that said means for recovery of said clock further comprises means for computing time differences between two consecutive arriving packets (20, 21, 23, 26), means for noise reduction (27, 52), a clock arranged to determine the rate for receiving packets, means for adjusting the frequency of said clock, a Mean estimator (28) and a Mean slope control block (33).

22. A packet-switched network according to claim 21, CHARACTERISED in that said Mean slope control block (33) comprises means for calculating the derivative (38) of the input data, said Mean slope control block (33) comprising means for adjusting (46) the period over which said Mean estimator (28) calculates mean values, and said Mean slope control block (33) comprising means for supplying (46) data to said means (34, 35) for adjusting said clock frequency (18).

23. A packet-switched network according to claim 21, CHARACTERISED in that said means for noise reduction (27) is a digital low pass filter (27, 52) with a period equal to the expected inter-arrival time, T_c.

24. A packet-switched network according to claim 21, CHARACTERISED in that said means for noise reduction (27) is a finite impulse response filter.

25. A packet-switched network according to claim 23, CHARACTERISED in that said digital low pass filter (27, 52) comprises a first low pass filter (47), a decimator (48) and a second low pass filter (49) and that said decimator (48) comprises means for supplying a clock signal (51) to said Mean estimator (28) and said Mean slope control block (33).

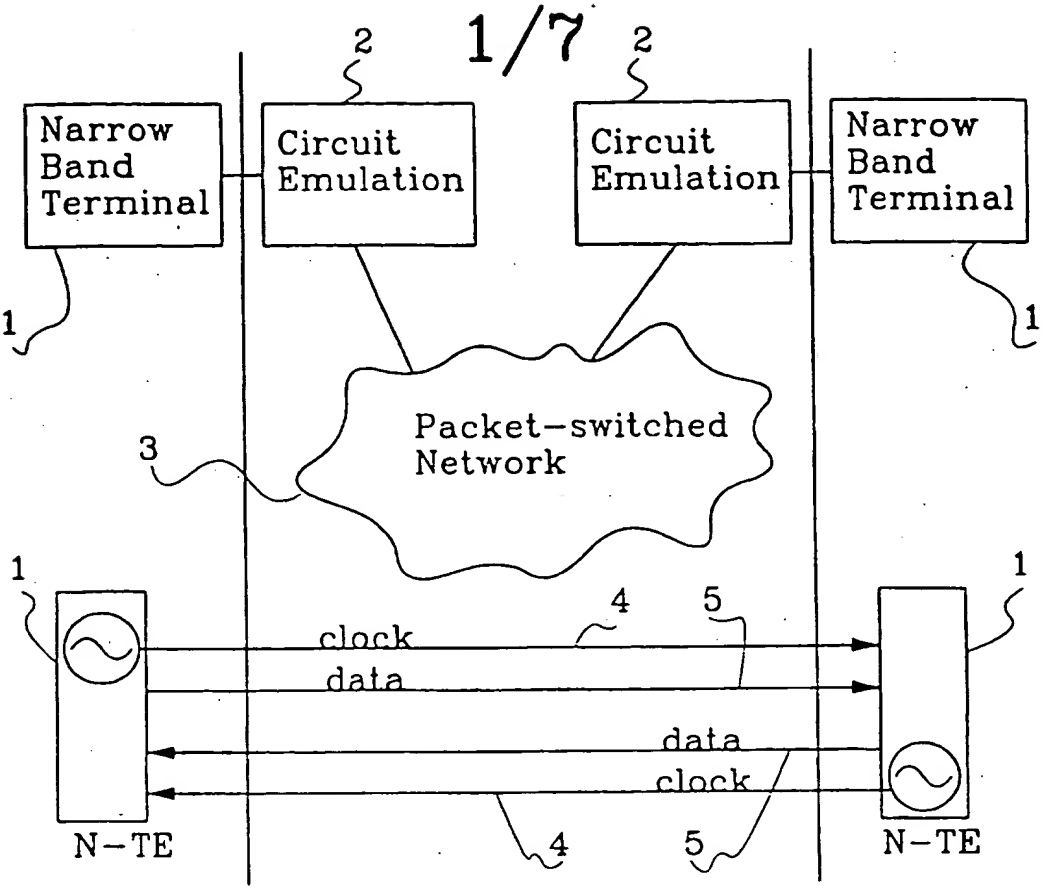
Narrow Band Terminal
Circuit Emulation
Circuit Emulation
Narrow Band Terminal
Packet-switched Network
clock
data
data
clock
N-TE
N-TE
1
2
2
3
4
5

FIG 1

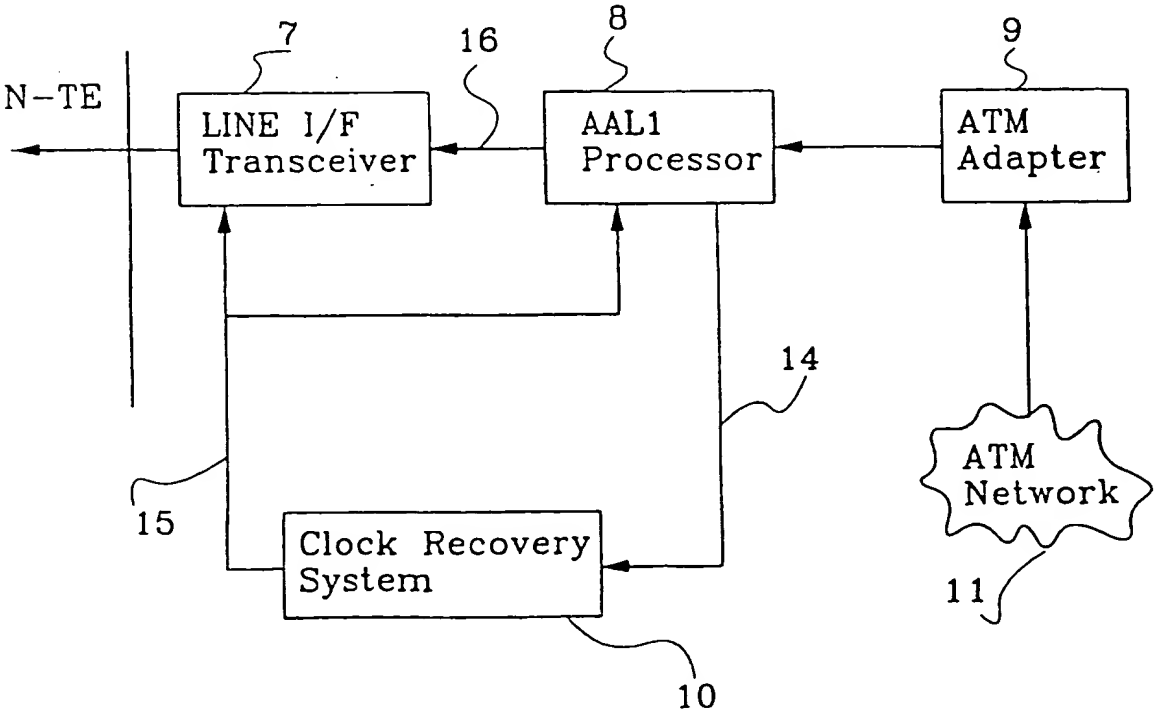
N-TE
LINE I/F Transceiver
AAL1 Processor
ATM Adapter
ATM Network
Clock Recovery System
7
8
9
16
14
15
10
11

FIG 2

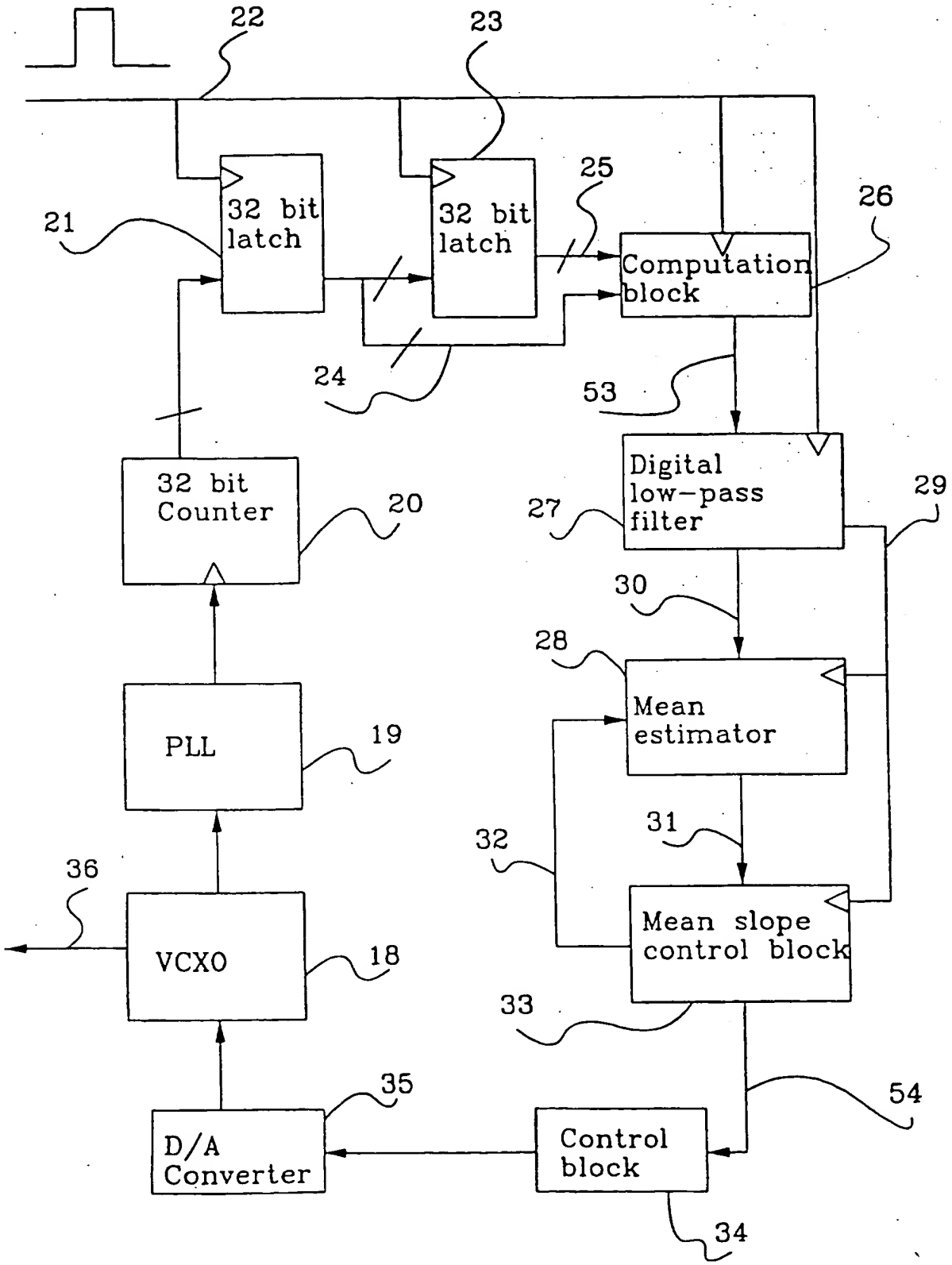
22
23
25
26
21
32 bit latch
32 bit latch
Computation block
24
53
Digital low-pass filter
29
27
32 bit Counter
20
30
28
Mean estimator
PLL
19
31
32
36
Mean slope control block
VCXO
18
33
35
54
D/A Converter
Control block
34

FIG 3

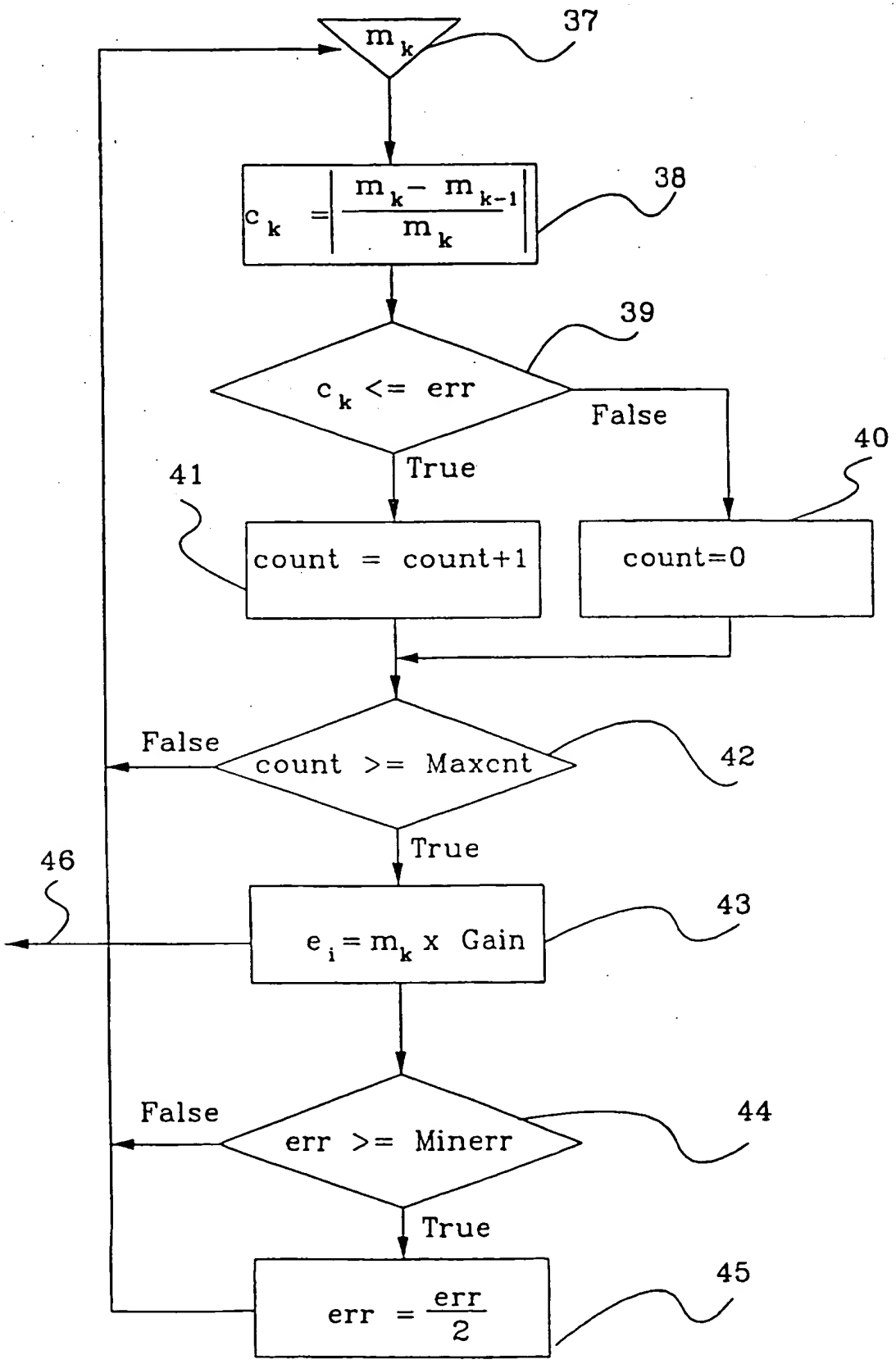
m_k
37
$c_k = \left| \frac{m_k - m_{k-1}}{m_k} \right|$
38
39
$c_k <= err$
False
True
40
41
count = count+1
count=0
False
count >= Maxcnt
42
True
46
$e_i = m_k \times Gain$
43
False
err >= Minerr
44
True
$err = \frac{err}{2}$
45

FIG 4

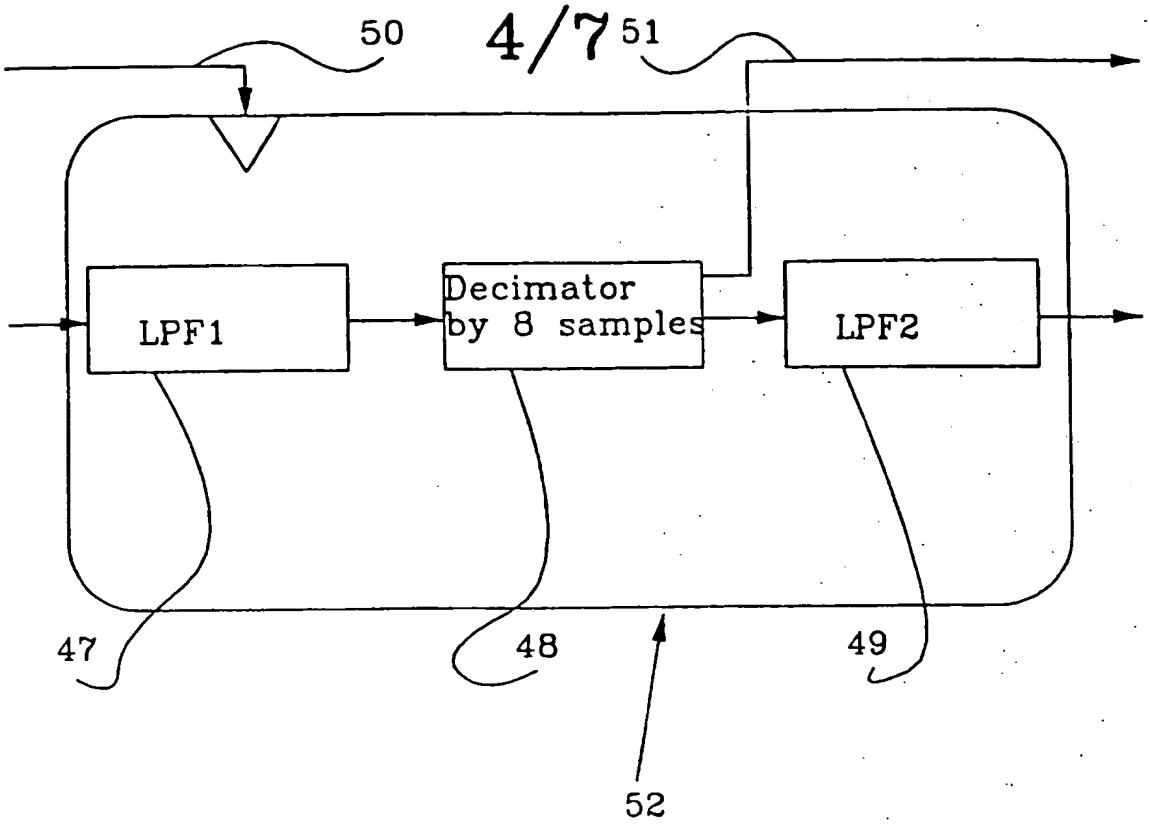

FIG 5

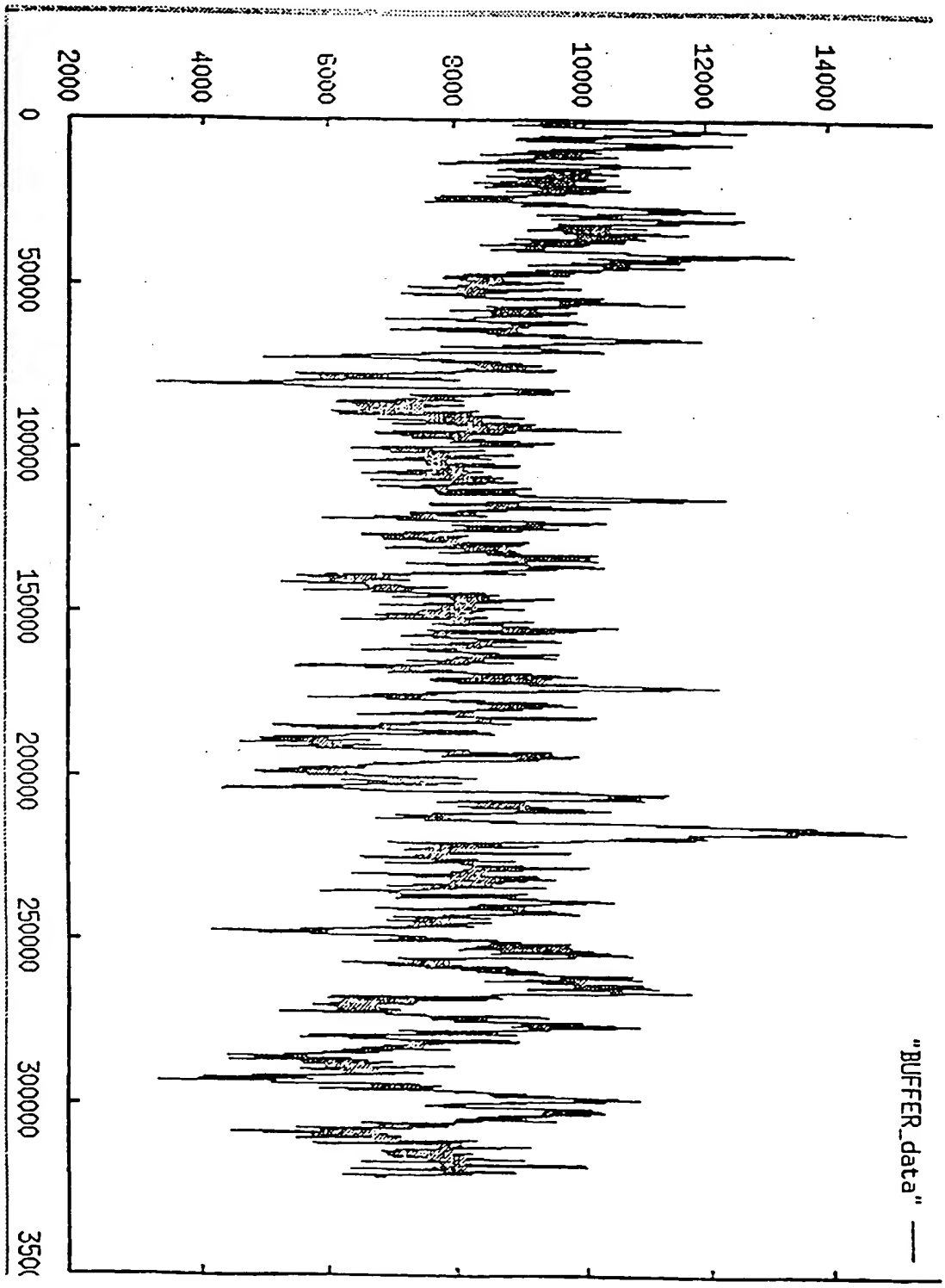
2000
4000
6000
8000
10000
12000
14000
0
50000
100000
150000
200000
250000
300000
350(
"BUFFER_data"

FIG 6

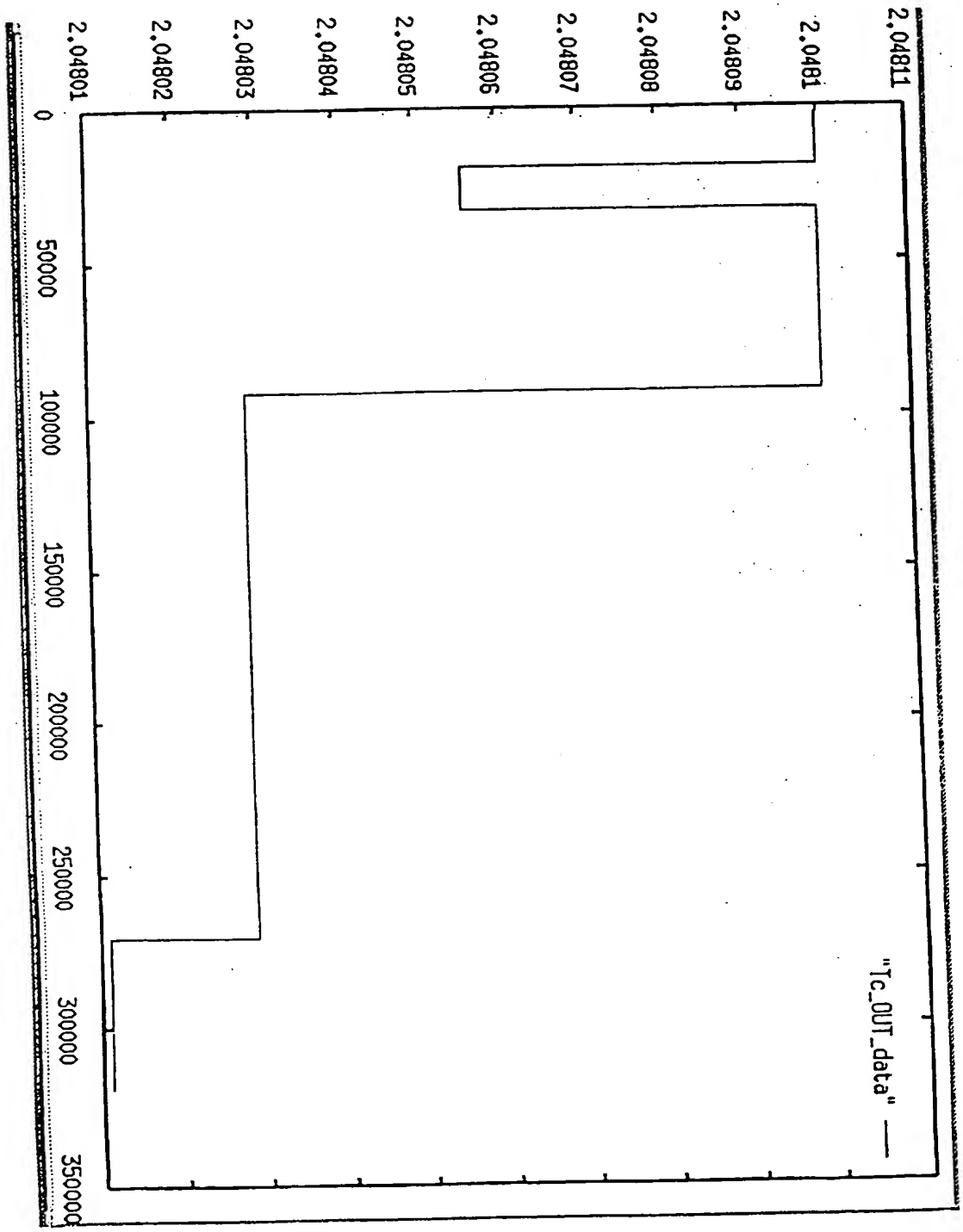
2.04811
2.0481
2.04809
2.04808
2.04807
2.04806
2.04805
2.04804
2.04803
2.04802
2.04801
0
50000
100000
150000
200000
250000
300000
350000
"Tc_OUT_data"

FIG 7

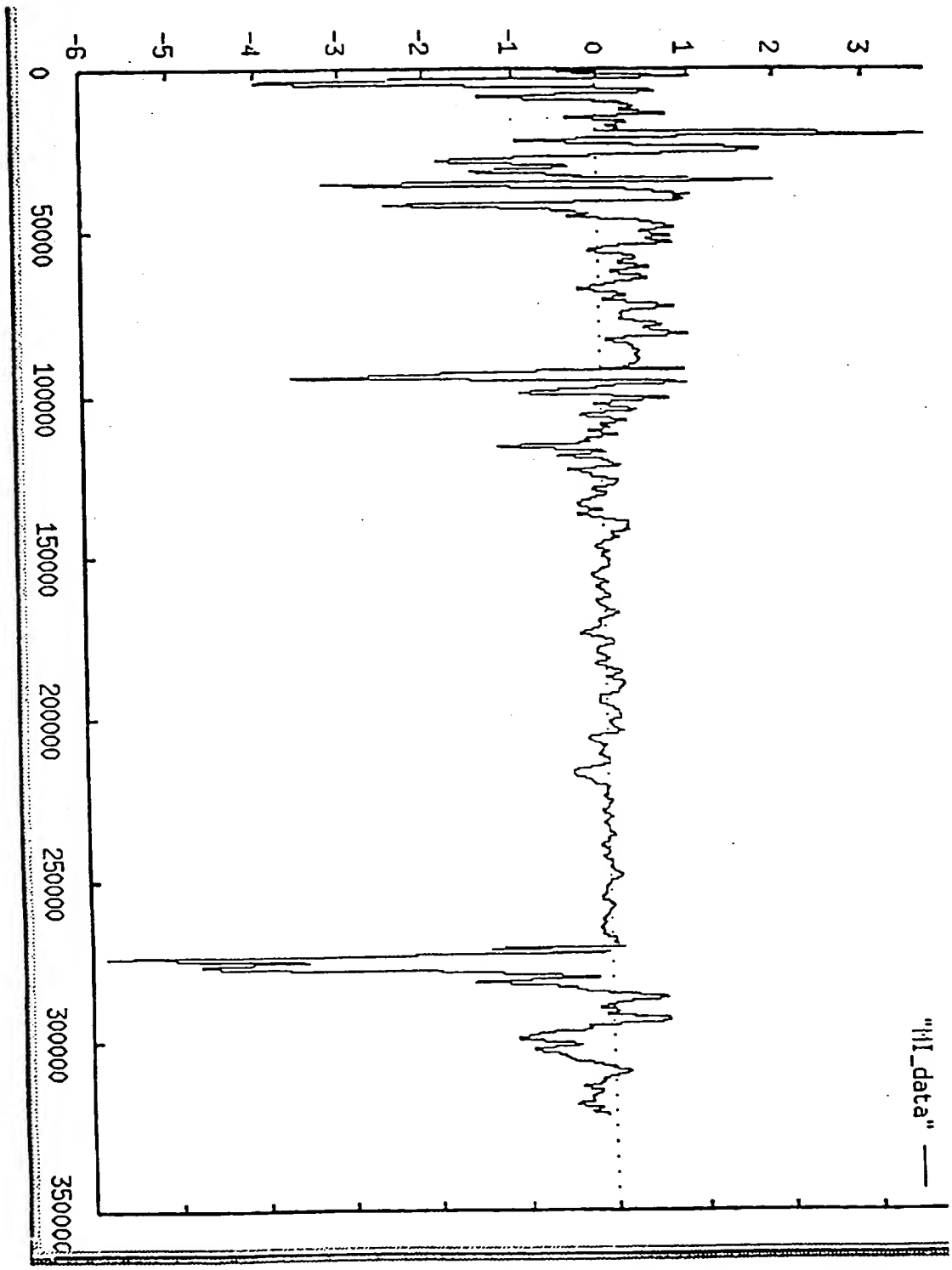
-6
-5
-4
-3
-2
-1
0
1
2
3
0
50000
100000
150000
200000
250000
300000
350000
"II_data"

FIG 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 97/01168

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H04L 7/00, H04L 7/02
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPIL, INSPEC, TDB, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	Lorne Mason, "Broadband Communications Global infrastructure for the information age", 1996, Chapman & Hall, (Canada), page 618-page 620 --	1-25
Y	BT Technolog J, Volume 13, No 3, July 1995, M Mulvet et al, "Timing issue of constant bit rate services over ATM" page 41-page 44 --	1-25
A	US 5425061 A (FRANK L. LACZKO, SR. ET AL), 13 June 1995 (13.06.95), column 2, line 40 - line 60; column 1, line 40 - line 65; column 4, line 50 - line 65, abstract --	1-25

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" erlier document but published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
8 January 1998	22 -01- 1998
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Linus Wretblad Telephone No. +46 8 782 25 00

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 97/01168

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	FR 536069 A1 (ALCATEL CIT), 7 April 1993 (07.04.93), column 1, line 30 - line 50; column 4, line 30 - line 50; column 7, line 10 - line 30 --	1-25
A	EP 0705051 A1 (KONINKLIJKE PTT NEDERLAND N.V.), 3 April 1996 (03.04.96), column 2, line 17 - line 45, abstract --	1-25
A	JP 7066814 A (ANRITSU CORP), 10 March 1995 (10.03.95), abstract, see the figure -- --------	1-2,15-16,21

INTERNATIONAL SEARCH REPORT

Information on patent family members

02/12/97

International application No.
PCT/SE 97/01168

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5425061 A	13/06/95	JP 7254895 A	03/10/95
FR 536069 A1	07/04/93	NONE	
EP 0705051 A1	03/04/96	CA 2158531 A	22/03/96
		JP 8111685 A	30/04/96
		NL 9401525 A	01/05/96
JP 7066814 A	10/03/95	NONE	